Notice of References Cited	Application/Control No. 10/773,058	Applicant(s)/Patent Under Reexamination KUCUKCAKAR ET AL.	
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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-4,589,052 A	05-1986	Dougherty, John J.	361/94
*	B	US-4,924,430 A	05-1990	Zasio et al.	716/6
*	C	US-5,095,454 A	03-1992	Huang, Chi-Lai	703/19
*	D	US-5,579,510 A	11-1996	Wang et al.	716/6
*	E	US-5,650,938 A	07-1997	Bootehsaz et al.	716/6
*	F	US-5,872,717 A	02-1999	Yu et al.	716/6
*	G	US-5,946,475 A	08-1999	Burks et al.	716/6
*	H	US-6,083,273 A	07-2000	Takeuchi, Hideki	716/6
*	I	US-6,327,557 B1	12-2001	Croix, John Francis	703/14
*	J	US-2002/0070775 A1	06-2002	Chiu, You-Ming	327/141
*	K	US-6,415,402 B2	07-2002	Bishop et al.	714/724
*	L	US-2003/0009318 A1	01-2003	Amatangelo et al.	703/19
*	M	US-2003/0237067 A1	12-2003	Mielke et al.	716/6

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
*	U	Schulz, Steven. 'Focus Reports: Timing Analysis' EETimes Online, 2000.
*	V	Ernst et al. "Razor: A Low-Power Pipleline Based on Circuit-Level Timing Speculation". Proceedings of the 36th International Symposium on Microarchitecture: IEEE 2003.
	W	Chen et al. "A New Framework for Static Timing Analysis, Incremental Timing Refinement, and Timing Simulation" IEEE 2000.
	X	Reorda et al. "Fault List Compaction through Static Timing Analysis for Efficient Fault Injection Experiments" Proceedings of the 17th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, 2002 IEEE.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 10/773,058	Applicant(s)/Patent Under Reexamination KUCUKCAKAR ET AL.	
	Examiner SHAMBHAVI PATEL	Art Unit 2128	Page 2 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2004/0044976	03-2004	Schultz, Richard	716/006
*	B	US-2004/0221252 A1	11-2004	Lichtensteiger et al.	716/006
*	C	US-2005/0065765 A1	03-2005	Visweswariah, Chandramouli	703/019
*	D	US-6,925,621 B2	08-2005	Mielke et al.	716/6
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Franzini et al. "Crosstalk Aware Static Timing Analysis: a Two Step Approach", IEEE.
	V	Hu, et al. "A Static Timing Analysis Environment Using Java Architecture for Safety Critical Real-Time Systems" Proceedings of the Seventh International Workshop on Object-Oriented Real-Time Dependable Systems, 2002 IEEE.
	W	Chapman, et al. "Combining Static Worst-Case Timing Analysis and Program Proof", Real-Time Systems, 1996.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.